The Claims:

This listing of the claims replaces all prior versions and listing of the claims in the present application.

Listing of Claims:

1-17. (canceled)

18. (previously presented) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board; and

buffer layer means having a first surface in contact with said second surface of said interconnection board and a second surface on which at least one external electrode is provided, said buffer layer means for providing at least one electrical contact between said one external electrode pad and said at least one external electrode and for absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.

19. (original) The semiconductor device as claimed in claim 18, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

20. (original) The semiconductor device as claimed in claim 18, wherein said at least external electrode comprises plural external electrodes.

21. (original) The semiconductor device as claimed in claim 18, wherein said external electrode comprises a solder ball.

22-26. (canceled)

27. (previously presented) The semiconductor device as claimed in claim 18, wherein said buffer layer means comprises:

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode.

28. (original) The semiconductor device as claimed in claim 27, wherein said plural generally column shaped electrically conductive layers are made of a metal.

29. (previously presented) The semiconductor device as claimed in claim 18, wherein said buffer layer means comprises:

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external

electrode pad of said interconnection board and a second end directly fixed said external electrode; and

a stress absorption layer filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally column shaped electrically conductive layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

30. (original) The semiconductor device as claimed in claim 29, wherein said plural generally column shaped electrically conductive layers are made of a metal.

31. (original) The semiconductor device as claimed in claim 29, wherein said stress absorption layer is made of an organic insulative material.

32. (previously presented) The semiconductor as claimed in claim 18, wherein said buffer layer means comprises:

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode;

a supporting plate having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said

supporting plate and said second surface of said interconnection board; and

a supporting sealing resin material filling said interspace and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tight contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

33. (previously presented) The semiconductor device as claimed in claim 32, wherein said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

34. (original) The semiconductor device as claimed in claim 32, wherein said plural generally column shaped electrically conductive layers are made of a metal.

35. (original) The semiconductor device as claimed in claim 32, wherein said supporting sealing resin material is made of an organic insulative material.

36. (previously presented) The semiconductor device as claimed in claim 18, further comprising a supporting layer on said second surface of said buffer layer means for supporting said external electrode.

37. (previously presented) The semiconductor device as claimed in claim 36, wherein said supporting layer further comprises:

a supporting plate having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer means to form an inter-space between said supporting plate and said second surface of said buffer layer means; and

a supporting sealing resin material filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

38. (previously presented) The semiconductor device as claimed in claim 18, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

39. (original) The semiconductor device as claimed in claim 38, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

40. (original) The semiconductor device as claimed in claim 39, further comprising at least a heat spreader provided on said at least semiconductor chip.

41. (original) The semiconductor device as claimed in claim 38, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

42. (previously presented) The semiconductor device as claimed in claim 41, further comprising:

a stiffener spaced from at least one peripheral edge of said semiconductor chip; and

a heat spreader contacting said semiconductor chip and said stiffener.

43. (previously presented) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board;

a buffer layer having a first surface contacting said second surface of said interconnection board;

a supporting plate spaced from a second surface of said buffer layer and defining a gap between said second surface of

said buffer layer and said supporting plate, said supporting plate having plural holes therein;

at least one external electrode in one of said holes in said supporting plate and connected to said at least one external electrode pad through said buffer layer; and

a sealing resin in said gap and surrounding and supporting said at least one external electrode.

44. (canceled)

45. (previously presented) The semiconductor device as claimed in claim 43, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

46. (original) The semiconductor device as claimed in claim 45, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

47. (original) The semiconductor device as claimed in claim 46, further comprising at least a heat spreader provided on said at least semiconductor chip.

48. (original) The semiconductor device as claimed in claim 45, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

49. (previously presented) The semiconductor device as claimed in claim 48, further comprising:

a stiffener spaced from at least one peripheral edge of said semiconductor chip; and

a heat spreader contacting said semiconductor chip and said stiffener.

50. (previously presented) The semiconductor device as claimed in claim 43, wherein said buffer layer comprises plural generally column shaped electrically conductive layers that connect said at least one external electrode to said at least one external electrode pad; and

a supporting sealing resin material surrounding said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is in tight contact with said plural generally column shaped electrically conductive layers.

51. (previously presented) The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said at least one external electrode.

52. (original) The semiconductor device as claimed in claim 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. (original) The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is made of an organic insulative material.

54. (original) The semiconductor device as claimed in claim 43, wherein said external electrode comprises a solder ball.

55-85. (canceled)

86. (previously presented) A semiconductor device comprising:

a multilayer interconnection board having first and second surfaces;

an external electrode pad formed in a side of said second surface;

a semiconductor chip mounted in a side of said first surface;

a metallic post protruding from said external electrode pad;

a metallic frame formed in said side of said first surface to surround said metallic post, a gap being thereby formed between said metallic post and said metallic frame; and

a resin layer filling said gap.

87. (previously presented) The semiconductor device as claimed in claim 86, wherein said external electrode pad has an exposed surface forming a substantially flat plane with said second surface.

88. (previously presented) The semiconductor device as claimed in claim 86, wherein a height of said metallic post from

said second surface is substantially equal to a height of said metallic frame from said second surface.

89. (previously presented) The semiconductor device as claimed in claim 86, further comprising:

a solder ball connected to said metallic post;

a support plate provided on a surface of said resin layer and having a hole, in which said solder ball is inserted;

an inter-space being thereby formed between said solder ball and said hole; and

a resin material filling said inter-space.